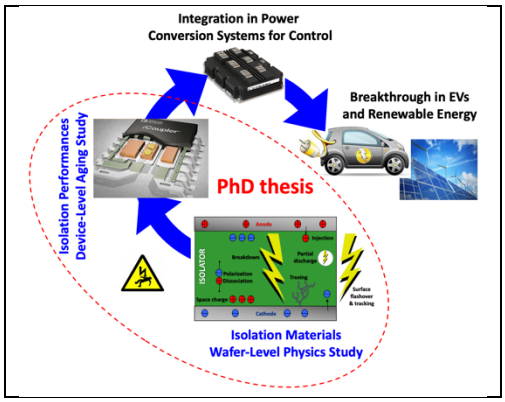
- PHD THESIS POSITION -

Electrical conduction and dielectric breakdown of thin insulating inorganic layers observed from nano- to micro-scales: Application to high voltage integrated isolation technology

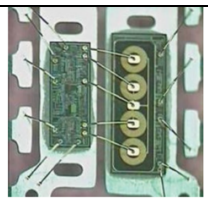
Context :

The acceleration of climate change pushes us to reduce of greenhouse gas emissions. As a result, faster development of transport electrification as well as greener energy production must continue. The transport electrification like electrical vehicules (EVs) have gained in popularity in recent years in an increasingly environmentally conscious society seeking to reduce CO_2 emissions. The electric motors in EVs fed by power inverters and powered by high-voltage batteries (mostly 400V today and higher tomorrow) contribute to considerably reducing these emissions. As battery voltage increases, electronic system and component suppliers must meet performance and safety challenges for these high power conversion applications to be released on the market. To increase battery efficiency, higher operating voltages are required, which poses two major challenges: power isolation and signal isolation for data communication. This revolution in sustainable transport will be made possible in particular by the new high-performance isolation gate-driver technologies to drive fast power devices (SiC or GaN) provided by digital isolators ensuring ultra-fast data transfer (>1Gb/s) through a thin dielectric barrier while guaranteeing insulation at high voltage. The current battery voltages (400V) will need to increase (>800V) and will require efficient and reliable isolation operating at 2000V.

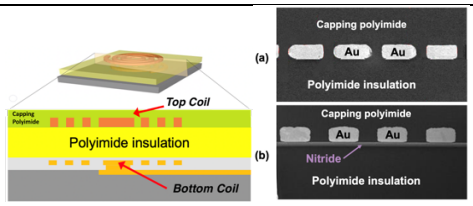


PhD Thesis Subject:

The thesis will aim to study and understand the mechanisms of high-field electrical conduction, pre-breakdown phenomena and dielectric breakdown of thin inorganic insulating layers (i.e. SiO_2, SiN_x, SiO_xN_y) used in organic polyimide-based digital isolators to sustain their rise in working voltage. The main objective will be to investigate the different macroscopic linear and nonlinear electrical conduction regimes of these different inorganic layers both in DC and in large-frequency AC voltage as a function of the applied electric field and temperature. Measurements will be achieved by using a high-voltage high-temperature 8-inches probe station to analyze the layers deposited on Si wafers in the form of metal-insulator-metal test structures (samples deposited and supplied in the cleanroom by our industrial partner). Correlations of the conduction properties with the physico-chemical and structuration properties will be carried out as a function of the deposition process parameters and layer thickness in order to optimize the electrical properties of the different materials. Moreover, pre-breakdown and breakdown mechanisms will be studied for each kind of materials and correlation with the conduction and structural properties will be analyzed.



Internal package view of a standard PI-based microtransformer isolator. [1]



Cross-section of a standard PI-based and PI-SiN_x-based micro-transformer isolator. [2]

[1] B. Chen and S. Diaham, "Polyimide Films for Digital Isolators", Chapter 6 in "Polyimide for Electronic and Electrical Engineering Applications", (Ed. S. Diaham, InTechOpen, London, UK, pp. 294, 2021).

[2] S. Diaham, L. O'Sullivan, E. Ceccarelli, P. Lambkin, J. O'Malley, J. Fitzgibbon, B. Stenson, P.J. Murphy, Y. Zhao, J. Cornett, A. Sow, B. Chen, and S. Geary. "Improving Polyimide Isolation Performance by Tailoring Interfaces with Nitride Layers for Digital Isolator Application." IEEE 3rd International Conference on Dielectrics (ICD), July 2020.

On another aspect of the thesis, measurement analyses between the macro-scale with nano-scale properties will be tempted by trying to setup 'on-chip' test structures to evaluate simultaneously the structural response of the materials (atomic network displacements observed by scanning transmission electron microscopy STEM) during the application of a high electric field. Such innovative in-situ experiments could enable to observe structural network movements of selected materials under strong field stimuli. A study of this impact jointly carried out at macroscopic scales (LAPLACE Institute, UPS, Univ. Toulouse, France) and at the nanometric scales (Univ. Limerick, Ireland) could enable to understand the various mechanisms of degradation (charge injection, conduction, space charge, breakdown) when the layers are gradually brought to their failure.

Working Program:
The thesis will be structured around 4 main areas of work:
- Definition of elementary electrical test structures for the electrical characterizations of the inorganic layers. All the samples will be processed in an industrial cleanroom by the Analog Devices company, Ireland (partnership during the thesis, https://www.analog.com/media/en/technical-documentation/tech-articles/polyimide-film-uses-for-digital-isolators.pdf).
- High voltage electrical characterization at the macroscopic scale using a HV probe station with multiple diagnostic techniques. Investigation of the structure/properties relationship.
- Design of test structures for STEM microscopy characterization: several measurement campaigns will be organized in the Univ. Limerick, Ireland, to study the degradation mechanisms at the sub-nanometer scale.
- Application of the study to the reliability evaluation of PI-based digital isolator test structures: the PhD student will work on accelerated electrical aging methodology (time-to-failure vs. voltage) on devices at wafer-level to evaluate new component designs for higher voltage reliability.

About LAPLACE Institute: http://www.laplace.univ-tlse.fr/?lang=en
The LAPLACE Institute, in the University of Toulouse – Paul Sabatier, seeks weave an "activity continuum" encompassing the production, the transportation, the management, the conversion and the use of the electricity while covering all the aspects right from the study of fundamental processes in solid and gas to the development of processes and systems. Within this widespread field, the major themes concern the plasma discharges as well as plasma applications, the study of the dielectric materials (polymers, in particular) and their integration into the systems, the study and the design of the electrical systems, the optimization of the control and the power converters. The research topics by their multidisciplinary nature lean on a physical science base willing to study the basic phenomena and introduce new concepts emanating from the fundamental sciences but, evidently, strongly motivated by the constraints and the technological or the environmental locks. They are therefore linked to the industrial activities through various collaborations and participate in the transfer of technologies, especially in the aeronautic, automotive and railway domains.

Expected PhD student profile:
• Master's degree (or equivalent engineering school's degree) in Electrical Engineering, Microelectronics, Material Sciences (with knowledge in physics of dielectrics).
• Skills in electrical characterizations (I-V, C-V, breakdown), structural characterizations (SEM, TEM, FIB, profilometry, AFM), physico-chemical characterizations (XPS, SIMS, EDX, FTIR …).
• Knowledge of microelectronic process technologies, charge injection/conduction theory, aging theory, interest in physical phenomena understanding.
• Software skills: LabView for electrical experiments automation, FEM for electrical field modeling (COMSOL).
• Good English level required (due to the international context of the thesis).
• Curiosity, rigor, team spirit, application, taste for practical work.

PhD thesis duration and starting date:
3 years starting from October 1st, 2022.

Location:
LAPLACE Institute
Université Paul Sabatier, Building 3R3
118 Route de Narbonne, F-31062 Toulouse, France.

Expected wages:
French governmental grant for 3 years around 25 k€ gross/year before income tax.

PhD Thesis Supervisor and contact to candidate:
Dr. Sombel Diaham, Associate Professor, LAPLACE, Université Paul Sabatier, sombel.diaham@laplace.univ-tlse.fr